International Journal of Electronics Communication and Computer Engineering
Volume 5, Issue 1, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

Analysis of Settling Time for Low Power CMOS Multistage Operational Amplifiers

Subodh Mahendre
University of RGPV Bhopal
Email: subhmahe@gmail.com

***Abstract* – Design procedure for multistage CMOS op-amp with features of fast settling and low power consumption is present in this paper. This method is focused on optimum compensation by means of proper placement of poles and zero. Single-stage cascode amplifier is no longer suitable in low-voltage designs. So that Multi-stage amplifiers are required with advance in technologies. To reduce the settling time and find the high gain in multi-stage Op-Amp, main aim is minimum mos used in this technology. Nested Miller compensation nulling-resistor technique is used. Simulations on a circuit implemented in a 0.35-µm technology closely to the results expected. Three stage op-amp circuits are simulated by Tanner tool. The results obtained by the circuit simulation are 163 nsec (Settling Time), 90dB (Gain), 9.3 V/µs (Slew Rate) and 11 MHz (Unity Gain Frequency).**

***Keywords* – CMOS, Multistage Amplifiers, Nested-Miller Compensation, Operational Transconductance Amplifiers (OTAs).**

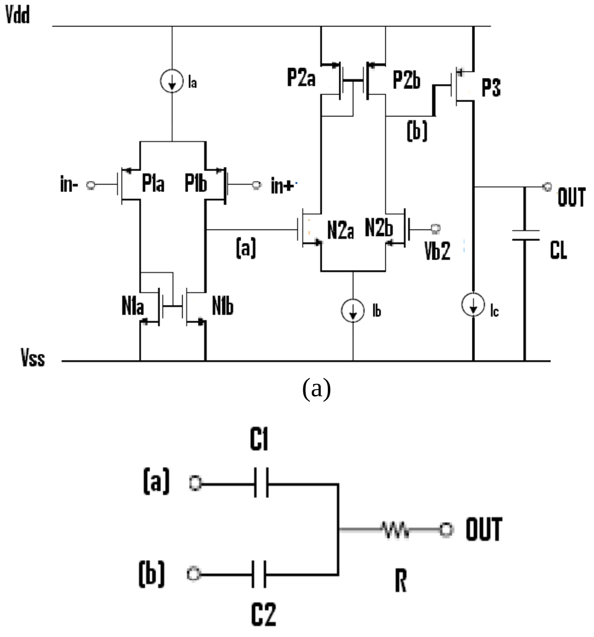
I. INTRODUCTION

The settling time of an op-amp is a very important parameter, particularly for switched-capacitor and data converter circuits. The settling time is defined to be the time takes for op-amp to reach a specified percentage of its final value, when a step input is applied. The total settling time can be broken up into two distinct regions; a slewing period (T_{SL}) and a settling period (T_{ST}). During the slewing period the output voltage changes from its original value to a voltage close to its final value and the op-amp operates in a rate limited fashion. And during the settling period the output voltage settles to its final value in a small-signal linear fashion. Low voltage, low power cmos multistage operational amplifier is to be designed with compensation technique on the consideration of settling time behavior. Multistage trans-conductance operational amplifiers (OTAs) are increasingly utilized by analog designers since they provide both high gain and voltage swing under reduced voltage supplies. In this paper, we shall describe a design procedure in which the aspect ratio of each transistor is related to the amplifier's main performance parameters. Aspect ratio of the each transistor is optimized according to their best performance. The approach is applied to a three-stage amplifier with low offset, high CMRR performance, high slew rate, high gain(>90 dB), high input impedance and minimum settling time.

The design considerations for fast-settling operational amplifiers (op-amps) are significantly different between sampled-data switched-capacitor (SC) and conventional continuous-time applications. This paper presents a multistage amplifier for low-voltage applications (<3V). For low voltage supply, multistage amplifier is designed in place of cascode amplifier. The goal of this work is to realize a multi-stage amplifier with a better bandwidth to power efficiency and suitable for driving high capacitive loads such as high accuracy sigma-delta modulators, pipeline A/D converters, linear regulators, and switch capacitors etc. System will be unstable in multistage amplifier design. So many compensation techniques are used to provide the stability, known as Miller compensation techniques. In this paper nested Miller compensation nulling-resistor technique is used to compensate the positive zero introduce in the circuit.

II. DESIGN PROCEDURE

The design procedure of three-stage amplifier is well known described in this paper. We shall describe a simple and well-defined design procedure in which the aspect ratio of each transistor is related to the amplifier's main performance parameters. Three-stage amplifier is designed on the basis of 0.35µm technology. The approach is based on the following main parameters: phase margin (m_{Φ}), gain-bandwidth product (f_{GBW}), load capacitance (C_L), slew rate (SR), input common mode range (CMR), input impedance and settling time. Important parameters such as DC gain, CMRR, will not be used during the design steps since they depend on the output resistance of MOS transistors that is not easily modeled.



(a)

(b)

Fig.1. Schematic of the three-stage CMOS OTA (a) and Compensation network (b).

The approach is applied to a three stage op-amp with low voltage, low power for good settling time performance. The circuit is made up of an input differential stage (transistors P1, N1 and current source), a second differential stage (P2, N2 and current source) and a final common-source stage (P3 and current source). Current source is further implemented by cmos current mirror. Parasitic capacitances will be neglected during design because they are much lower than compensation and load capacitances. Moreover, a pencil-and-paper design suggests how to perform modifications if targets have not been reached. By using the current equation W/L can be calculated for all the MOS transistors.

III. SIMULATION RESULTS

The design is simulated by Tanner tool, using the model parameters of a 0.35-µm double-metal double-poly process with transistors' threshold voltages of about 600mV. The following design parameters were assumed: VDD-VSS=2V, C_L=10pF, SR=10V/µs, f_{GBW}=10MHz, $m_{\varnothing}$=60°. We found current through the branches I_a=70µA, I_b=63µA and I_c=233µA. Moreover, we obtained $(W/L)_{P1a}=(W/L)_{P1b}=94/1$,$(W/L)_{N1a}=(W/L)_{N1b}=1.6/1$,$(W/L)_{N2a}=(W/L)_{N2b} = 45/1$, $(W/L)_{P2a} = (W/L)_{P2b} = 90/2$, $(W/L)_{P3} = 246/1$. Regarding the compensation network, we get C1=7pF, C2=5pF and R=550Ω. We simulated a first version of the circuit in Fig. 1 by using the above dimensions and IB=35µA. With these settings the following trans conductance values were found: gmP1=294µA/V, gmN1=58µA/V, gmN2=371µA/V and gmP3=1335µA/V, which, as expected, are different from those estimated by the procedure, causing the circuit's performance to deviate from specifications. Indeed, although the circuit exhibits a very low systematic input offset voltage equal

$$I_D = (1/2)\ \mu C_{OX}\,(W/L)\,(V_{GS} - V_T)^2 \quad .... (1)$$

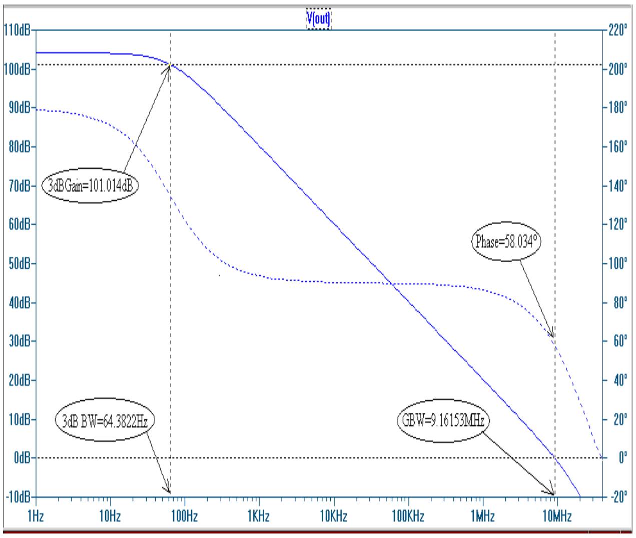


Fig.2. Gain and Phase plot of Op-amp

To design of three stage amplifier, the basic requirement is input resistance to be high and output resistance is less. Hence input differential stage is designed by pmos pair, because of resistance of pmos is very high as compare to nmos. In input differential stage nmos pair is used as current mirror. If both inputs are to be grounded, $I_a/2$ 10µV, the DC gain and gain-bandwidth product were 87dB and 6.4MHz, respectively with a phase margin of 60°. Positive and negative SR was 8.9V/µs and -9.5V/µs. In particular, the frequency response is illustrated in Fig. 2.

IV. CONCLUTION

Three-stage Operational Trans-conductance Amplifier has been designed in low-voltage environment. The main research efforts have been aimed on the frequency compensation task, which is perhaps the most difficult one, but that is only one of the several steps required to obtain a complete and efficient amplifier. Well-defined design strategy, closely meeting target specifications should be available. This thesis proposed design procedures for three-stage CMOS OTAs compensated with the simplest possible Nested Miller Compensation Nulling-Resistor technique. Simulated and experimental data from implementations designed in a 0.35-µm technology were found in a reasonable agreement with the results expected. In particular, the op-amp solution exhibits a gain-bandwidth product of 9.16MHz with a SR and settling time of 13V/µsec and 126.97ns, respectively, while dissipating 966µW

Table 1: Simulated Main Performances (Final Design)

Parameters of Op-amp	**Values**
Input Voltage Range	±5.8µV
Power Consumption	966µW
Gain	104dB
GBW	9.16MHz
Phase Margin	120°
Settling Time	126.97nsec
Slew Rate	13V/µsec
Capacitive Load	10pF

REFERENCES

[1] Ka Nang Leung and Philip K. T. Mok, "Analysis of Multistage Amplifier-Frequency Compensation,'' IEEE Transactions On Circuits And Systems—I: Fundamental Theory And Applications, Vol.48, No.9, September 2001.

[2] Bhupendra K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," IEEE Journal Of Solid-State Circuits, Vol. Sc-18, No. 6, December 1983.

[3] Feng Wang and Ramesh Harjani, "An Improved Model for the Slewing Behavior of Op-Amp," IEEE Transactions On Circuits And Systems-Ii: Analog And Digital Signal Processing, Vol.42, No.10, Oct-1995.

[4] G. Palmisano, G. Palumbo and S. Pennisi, "Design Procedure for Two-Stage CMOS Trans-conductance Operational Amplifiers," Analog Integrated Circuits and Signal Processing, 27, 179–189, 2001, Kluwer Academic Publishers. Manufactured in The Netherlands.

[5] Mohammad Yavari and Omid Shoaei, "Low-Voltage, Low-Power Fast-Settling CMOS Operational Trans-conductance Amplifiers for Switched-Capacitor Applications," IC Design Lab, ECE Department, University of Tehran, Tehran 14395-515, Iran, August 25-27,2003.

[6] Preetam Tadeparthy, “An Improved Frequency Compensation Technique for Low Power, Low Voltage CMOS Amplifiers,” Broadband Silicon Technology center, Texas Instruments India Ltd, Bangalore, India—2004 IEEE.

[7] G. Palumbo and S. Pennisi, “Design Guide-Line for Optimized Nested Miller Compensation” Mixed Signal Design, 2000, Ssmsd South-West Symposium On, 27-29 Feb-2000.

[8] Ka Nang Leung, Philip K. T. Mok, Wing-Hung Ki and Johnny K. O. Sin, “Three-Stage Large Capacitive Load Amplifier with Damping-Factor-Control Frequency Compensation,” IEEE Transactions On Solid-State Circuits, Vol. 35, No.2, February 2000.

[9] Ka Nang Leung and Philip K. T. Mok, “Nested Miller Compensation in Low-Power CMOS Design,” IEEE Transactions On Circuits And Systems—Ii: Analog And Digital Signal Processing, Vol.48, No.4, April 2001.

[10] Gaetano Palumbo and Salvatore Pennisi, “Design Methodology and Advances in Nested-Miller Compensation,” IEEE Transactions On Circuits And Systems—I: Fundamental Theory And Applications, Vol. 49, No. 7, July 2002.

[11] Rosario Mita, Gaetano Palumbo and Salvatore Pennisi, “Design Guidelines for Reversed Nested Miller Compensation in Three-Stage Amplifiers,” IEEE Transactions On Circuits And Systems—Ii: Analog And Digital Signal Processing, Vol. 50, No. 5, May 2003.

[12] R. Mita, G. Palumbo and S. Pennisi, “Well-Defined Design Procedure for a Three-Stage CMOS OTA,” IEEE International Symposium On, Circuits & Systems, Vol.-3, May-2005.

[13] D. Grasso, R. Mita, G. Palumbo and S. Pennisi, “Design Procedures for Three-Stage CMOS OTAs with Nested-Miller Compensation,” IEEE Transactions On Circuits And Systems—I: Regular Papers, Vol. 54, No.5, And May 2007.

[14] Majid Jalalifar, Mohammad Yavari and Farshid Raissi, “A Novel Topology in Reversed Nested Miller Compensation Using Dual-Active Capacitance,” Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran, IEEE, 2008

[15] Siroos Araghian Abbas Golmakani A Novel Low Power Topology in Reversed Nested Miller Compensation Using Triple-Active Capacitance Volume 2 Issue 6 (November 2012)

[16] Sau Siong Chong, and Pak Kwong Chan, Cross Feedforward Cascode Compensation for Low-Power Three-Stage Amplifier With Large Capacitive Load Solid-State Circuits, Vol. 47, No. 9, September 2012

[17] Andrea Pugliese, Francesco Antonio Amoroso,Gregorio Cappuccino, and Giuseppe Cocorullo Corrections to“Settling Time Optimization for Three-Stage CMOS Amplifier Topologies Transactions On Circuits And Systems—I: Regular Papers, Vol. 57, No. 7, July 2010

[18] Ray Nguyen, and Boris Murmann,The Design of Fast-Settling Three-Stage Amplifiers Using the Open-Loop Damping Factor as a Design Parameter Transactions On Circuits And Systems—I: Regular Papers, Vol. 57, No. 6, June 2010

[19] Song Guo,and Hoi Lee,Dual Active-Capacitive -Feedback Compensation for Low-Power Large-Capacitive-Load Three-Stage Amplifiers Solid-State Circuits, Vol. 46, No. 2, February 2011

[20] Punith R. Surkanti, Student Member, IEEE, and Paul M. Furth, Senior Member, IEEE Converting a Three-Stage Pseudoclass-AB Amplifier to a True-Class-AB Amplifier Circuits And Systems—Ii: Express Briefs, Vol. 59, No. 4, April 2012

AUTHOR’S PROFILE

Subodh Mahendre

was born in 1987 in betul(mp india) my BE (TIETECH JABALPUR) and Mtech(TIT BHOPAL) degree both from university of RGPV BHOPAL lin 2010 AND 2013 , my BE degree in eelectronic and communication engineering and Mtech degree in Micro Elelctronics & VLSI Design His primary research interests include bipolar and CMOS high performance digital circuits, low-power multistage amplifiers and this research is gain and phase plot.